4 GHz 3 WATTS FET AMPLIFIER FOR DIGITAL TRANSMISSION

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ABSTRACT

A 4 GHz high power FET amplifier for digital transmission is presented. The four-stage amplifier is composed of six amplifier-modules, and has 3 W output with 25 dB gain in linear operation and 6 W output with 22 dB at saturation over the 3.7-4.2 GHz range. In 45 Mbit/sec 8-PSK signal transmission, this amplifier shows approximately 0.1 dB degradation in C/N.

Introduction

Recently, microwave Gallium Arsenide Schottky-barrier gate field effect transistors (GaAs FETs) have gaind acceptance as high power amplifiers for TWT-replacement. High power application in an FM radio relay system in C band[1] and third order intermodulation distortion of GaAs FETs in X band[2] have been reported previously.

This paper describes a 4 GHz 3 W GaAs FET linear amplifier for digital transmission. The amplifier consists of six amplifier-modules which are matched to 50-Ω lines at input and output ports.

In 45 Mbit/sec 8-PSK signal transmission, C/N degradation due to this amplifier is approximately 0.1 dB at bit-error-rate of 10^{-6}.

Design

Figure 1 is the block diagram of the four-stage amplifier. The first and third stages are single amplifier-modules; the second and fourth stages use two modules in parallel.

Amplifier-module

An amplifier-module consists of a commom sourced FET and alumina ceramic substrates, on which input/output impedance matching networks and DC bias circuits are integrated, on a copper plate as shown in Fig. 2. Figure 3 shows the equivalent circuit. The impedance matching network at the output port is designed to give maximum power output at the 1-dB gain compression point. The bias choke circuits include 50-Ω resistors (R_1, R_2). These resistors furnish the resistive load for FET, especially at lower frequencies of the out-band, and result in unconditionally stable operation of the module.

The modules are individually adjusted in a test mount, to provide the best linearity and amplitude response. Particularly, the transmission phase difference between modules which operate in parallel has been tuned within 10-degrees over the band to minimize combined power loss.

Four stage amplifier

The optimum power matching load impedance of FET is different from its small signal impedance $(S11^*)$[3]. When the modules operate in cascade directly, the amplitude response changes according to operating level. Therefore, in this amplifier, hybrid couplers are inserted between single and parallel stages to minimize the influence of impedance deviation of FET. as a rasult, the amplifier shows good linearity and high saturation output power throughout the frequency band.

As shown in Fig. 3, the modules are mounted on one side of the housing. The hybrids and power supply are on the opposite side of the housing, as shown in Fig. 5. Repairs can be made quickly and conveniently by replacing modules.

The FET modules require both positive and negative voltage. The +12 V input is dropped and regulated at 10 V for the drain supply, and is converted to a -6 V gate bias supply by a DC-DC converter.

Performance

Typical characteristics of the amplifier-modules are as follows:

	CG0401	CG0402
Frequency range	: 3.7-4.2 GHz	3.7-4.2 GHz
Output power (1-dB comp.)	: 0.6 W	2.5 W
Power gain (")	: 8 dB	5 dB
Saturated output power	: 0.9 W	4 W
Efficiency	: 30 %	30 %
Input/Output VSWR.	: 2.0/2.0	3.0/2.0

Figure 6 shows typical input and output impedance loci of the CG0402.

Typical performance of the four stage amplifier is as follows:

Frequency range	: 3.7-4.2 GHz
Output power (linear/saturation)	: 3/6 W
Power gain (" / ")	: 25/22 dB
3rd IM intercept point	: 50 dBm
Noise figure	: 8 dB
AM-PM conversion (at 1-dB comp.)	: 1 deg./dB
Power requirment	: +12 V, 3 A

Figure 7 shows the output power and AM-PM conversion versus input level and Figure 8 shows the amplitude frequency response.

This amplifier has been tested for digital transmission of 45 Mbit/sec 8-PSK signal. The BER test setup and results are shown in Fig. 9. The transmitter and receiver filters are as follows.

Transmitter	: Transversal type cosine roll off (K=0.7) with amplitude equalizer in base band frequency
Receiver	: 4-section Butterworth in IF (BT=1.2)

In this experiment, C/N degradation due to the amplifier is about 0.1 dB at BER 10^{-6} point with 3 W output linear operation, and 0.6 dB with 6 W output saturated operation. Figure 10 shows the power spectrum of PSK signal at the output of the amplifier at 3 W. The excess spurious emission due to third order intermodulation can be suppressed by a 5 or 6-section filter with 30 MHz band width (BT=2.0). This filter does not degrade BER of 45 Mbit/sec 8-PSK signal.

The FM 1800 channel noise loading test was also carried out at 6 W output level. The noise from the amplifier was less than 2 pWop at the top channel.

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Conclusions

The design and performance of a 4 GHz band GaAs FET high power amplifier for digital transmission have been described. Production and maintenance of this amplifier are simplified by the use of amplifier-modules.

The amplifier provides good performance characteristics for digital transmission and low spurious emission caused by nonlinearity, and is compatible with FM and PSK signal applications.

Acknowledgement

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References

1) H. Komizo, et al, "A 7 GHz FM Transmission Utilizing GaAs Power MESFETs", pp 243-245, 1977 IEEE-MTT-S International Microwave Symposium.

2) H.Q. Tserng, et al, "X-Band MIC GaAs FET Power Amplifier", pp 101-103, 1976 IEEE-MTT-S International Microwave Symposium.

3) Y. Takayama, "A New Load-Pull Characterization Method For Microwave Power Transistor", pp 218-220, 1976 IEEE-MTT-S International Microwave Symposium.

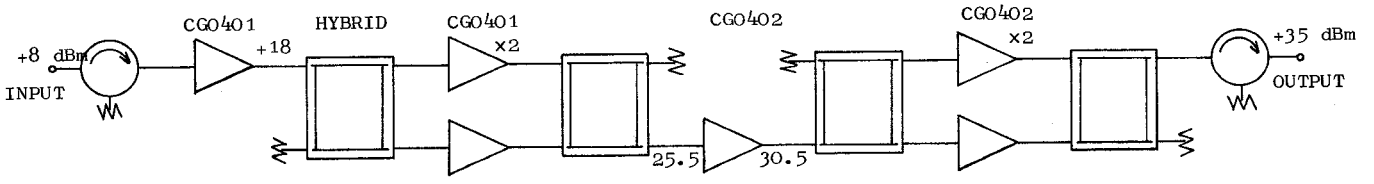

Fig. 1 Block diagram.

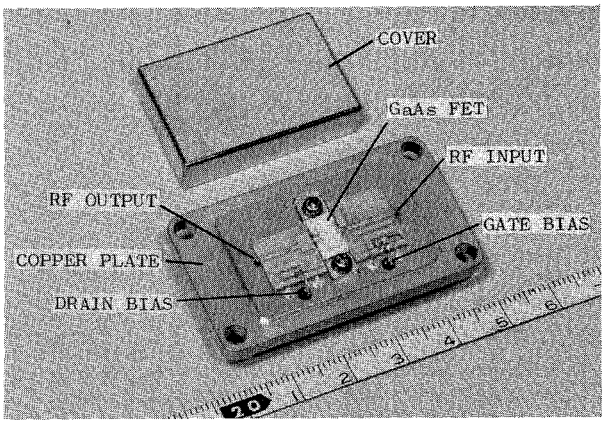

Fig. 2 Amplifier-module.

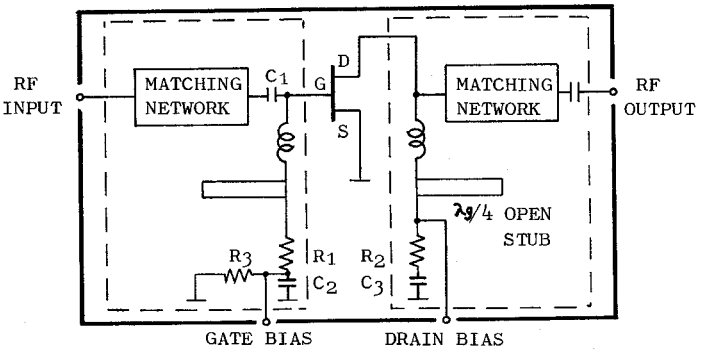

Fig. 3 Equivalent circuit of the module.

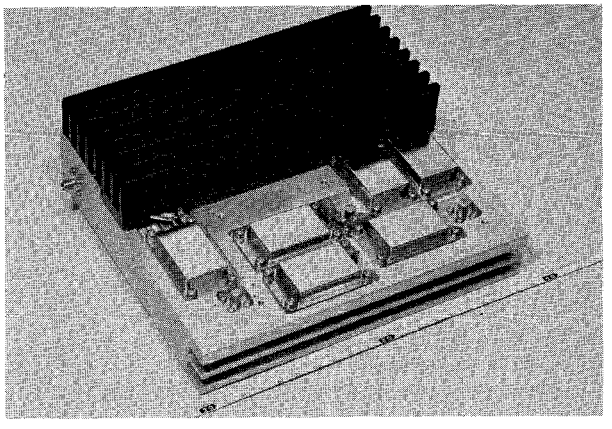

Fig. 4 Module side view of the amplifier.

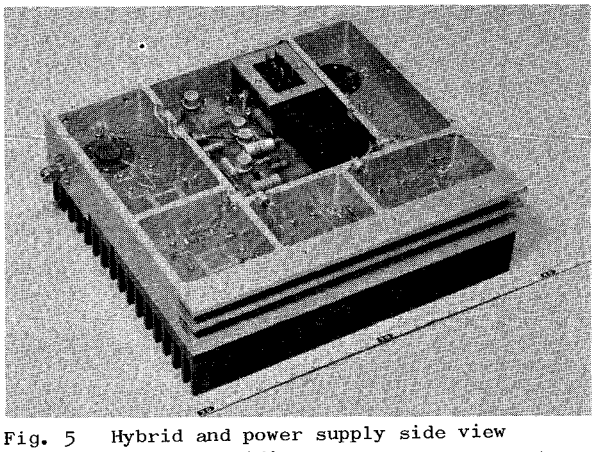

Fig. 5 Hybrid and power supply side view of the amplifier.

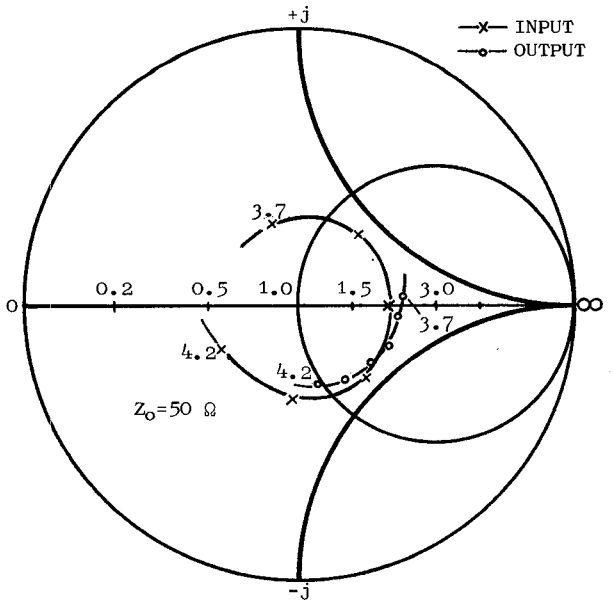

Fig. 6 Input and output impedance loci of CG0402.

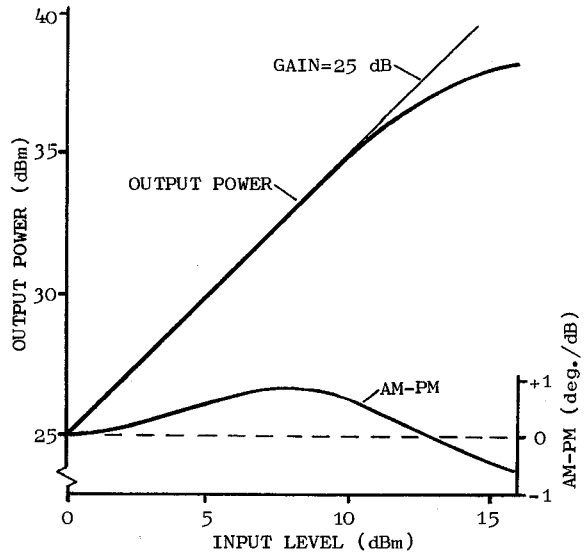

Fig. 7 Output power and AM-PM conversion versus input level.

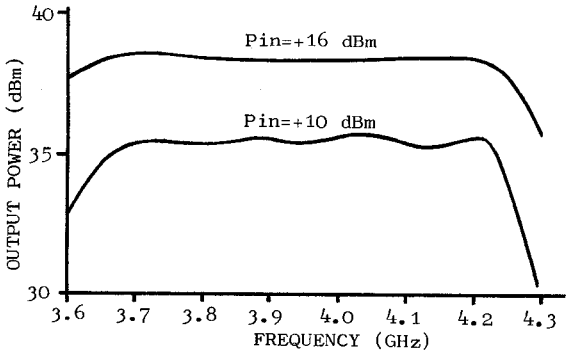

Fig. 8 Amplitude frequency response.

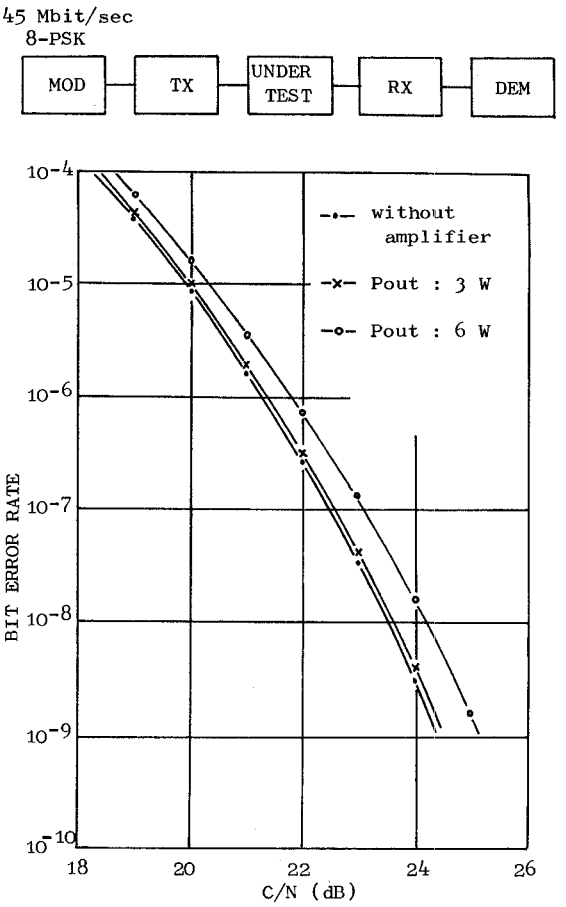

Fig. 9 Bit error rate and test setup.

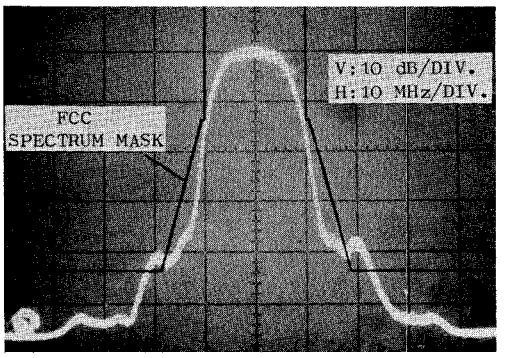

Fig. 10 Power spectrum.